Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, the assembly comprising:

~~the assembly comprising:~~

a peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in actual operation;

~~a plurality of clock generators to generate clocks asynchronous with each other and to supply the clocks to the target LSI; and~~

a first clock generator for generating a first clock as a reference clock for the actual operation in the target LSI;

a second clock generator for generating a second clock to allow the target LSI to obtain the test signal from the LSI tester;

a third clock generator for generating a third clock to allow the target LSI to output a test result signal, wherein the first clock, the second clock, and the third clock are asynchronous with each other; and

a printed circuit board on which the peripheral circuit and the ~~plurality of~~ first, second, and third clock generators are mounted.

2. (Original) The assembly for an LSI test of claim 1, including:

a first board including the peripheral circuit and the printed circuit board; and

a second board coupled to the first board and including wiring for coupling the first board and the LSI tester to each other.

3. (Original) The assembly for an LSI test of claim 1, wherein the test signal is supplied to the peripheral circuit and then output from the peripheral circuit to the target LSI.

4. (Original) The assembly for an LSI test of claim 1, wherein the test result signal is supplied to the peripheral circuit and then output from the peripheral circuit to the LSI tester.

5. (Currently Amended) The assembly for an LSI test of claim 1, wherein a memory is provided as the peripheral circuit or in the target LSI, and the LSI tester is configured to be capable of accessing the memory asynchronously to a clock supplied to the target LSI

~~the LSI tester is configured to be capable of accessing the memory asynchronously to a clock supplied to the target LSI~~.

6. (Original) The assembly for an LSI test of claim 5, wherein the test signal is stored in the memory, and then read out from the memory to be processed by the target LSI.

7. (Original) The assembly for an LSI test of claim 5, wherein the test result signal is stored in the memory, and then read out from the memory to the LSI tester.

8. (Currently Amended) An assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, the assembly comprising:

~~the assembly comprising:~~

a test result receiving circuit for performing given processing on data obtained as the test result signal so as to reduce the amount of the data, and for outputting a result of the processing to the LSI tester;

~~a plurality of clock generators to generate clocks asynchronous with each other and to supply the clocks to the target LSI; and~~

a first clock generator for generating a first clock as a reference clock for the actual operation in the target LSI;

a second clock generator for generating a second clock to allow the target LSI to obtain the test signal from the LSI tester;

a third clock generator for generating a third clock to allow the target LSI to output a test result signal, wherein the first clock, the second clock, and the third clock are asynchronous with each other; and

a printed circuit board on which the test result receiving circuit and the ~~plurality of~~ first, second, and third clock generators are mounted.

9. (Original) The assembly for an LSI test of claim 8, wherein an enable control circuit for selecting necessary data from the data obtained as the test result signal and for outputting the selected data is provided in the test result receiving circuit or in the target LSI.

10. (Original) The assembly for an LSI test of claim 8, wherein the test result receiving circuit includes a compression circuit for compressing input data and outputting the compressed data.

11. (Original) The assembly for an LSI test of claim 8, wherein the test result receiving circuit includes a determination circuit for determining whether or not the input data coincides with data to be input when the target LSI operates normally, and outputting a result of the determination.

12. (Currently Amended) An LSI test system, comprising:

an LSI tester for supplying a test signal to a target LSI to be tested; and

an assembly for an LSI test which outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, wherein the assembly comprises:

a peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in actual operation;

a first clock generator for generating a first clock as a reference clock for the actual operation in the target LSI;

a second clock generator for generating a second clock to allow the target LSI to obtain the test signal from the LSI tester;

a third clock generator for generating a third clock to allow the target LSI to output a test result signal, wherein the first clock, the second clock, and the third clock are asynchronous with each other; and

a printed circuit board on which the peripheral circuit and the first, second, and third clock generators are mounted

~~wherein the assembly comprises,~~

~~a peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in actual operation;~~

~~a plurality of clock generators to generate clocks asynchronous with each other and to supply the clocks to the target LSI; and~~

~~a printed circuit board on which the peripheral circuit and the plurality of clock generators are mounted~~.

13. (Currently Amended) An LSI test method, comprising the steps of:

operating a non-defective LSI, which is configured as a target LSI to be tested and has been confirmed to operate normally, in a circuit equivalent to a circuit actually used, and generating and storing a test signal and a reference test result signal, based on a signal supplied to the non-defective LSI and a signal output from the non-defective LSI, respectively, wherein the circuit comprises a first clock generator for generating a first clock as a reference clock for the actual operation in the target LSI, a second clock generator for generating a second clock to allow the target LSI to obtain the test signal, and a third clock generator for generating a third clock to allow the target LSI to output a test result signal, wherein the first clock, the second

clock, and the third clock are asynchronous with each other ~~a plurality of clock generators to generate clocks asynchronous with each other and to supply the clocks to the target LSI~~;

supplying the test signal to the target LSI synchronized with the second clock ~~a first one of the clocks~~;

carrying out the actual operation for the target LSI synchronized with the first clock ~~a second one of the clocks~~;

outputting the test result signal from the target LSI synchronized with the third clock ~~a third one of the clocks~~; and

determining whether or not the target LSI is defective by comparing the test result signal with the reference test result signal.

14-16. (Cancelled)